LISTING OF CLAIMS

Claims 1-14. (Canceled)

15. (Currently Amended) A circuit, comprising:

a pixel sensor;

a transistor coupling the pixel sensor to a bit line;

a first sampling capacitor selectively coupled to the bit line;

a second sampling capacitor selectively coupled to the bit line;

a bias current generator selectively coupled to the bit line;

a control circuit which operates ~~operable~~ to selectively couple the bit line to the first sampling capacitor during a first sample period and selectively couple the bit line to the second sampling capacitor during a second sample period, the control circuit further operable, during each of the first and second sample periods, to selectively couple the bias current generator to the bit line to bias the transistor into a follower configuration.

16. (Original) The circuit of claim 15 wherein the control circuit selectively couples the bias current generator to the bit line at a beginning of each of the first and second sample periods.

17. (Original) The circuit of claim 16 wherein the control circuit de-couples the selectively coupled bias current generator from the bit line before an end of each of the first and second sample periods.

18. (Original) The circuit of claim 17, wherein each first and second sampling period is of the order of one microsecond, and a duration of the selective coupling of the bias current generator is of the order of 100 nanoseconds.

Claims 19-25. (Canceled).

26. (Currently Amended) A circuit, comprising:

a pixel sensor;

a transistor coupling the pixel sensor to a bit line;

a sampling capacitor selectively coupled to the bit line;

a bias current generator selectively coupled to the bit line;

a control circuit which operates ~~operable~~ to selectively couple the bit line to the sampling capacitor during a sample period, the control circuit further operable to selectively couple the bias current generator during the sample period to the bit line to bias the transistor into a follower configuration.

27. (Original) The circuit of claim 26 wherein the control circuit selectively couples the bias current generator to the bit line at a beginning of the sample period.

28. (Original) The circuit of claim 27 wherein the control circuit de-couples the selectively coupled bias current generator from the bit line before an end of the sample period.

29. (Original) The circuit of claim 28, wherein the sampling period is of the order of one microsecond, and a duration of the selective coupling of the bias current generator is of the order of 100 nanoseconds.

30. (New) The circuit of claim 15, wherein during the first sample period a first non-zero level of pixel voltage is applied to a gate of the transistor biased in the follower

configuration, and wherein during the second sample period a second non-zero level of pixel voltage, different from the first level of pixel voltage, is applied to the gate of the transistor biased in the follower configuration.

31. (New) The circuit of claim 15, wherein the control circuit operating to selectively couple the bias current generator to the bit line further comprises operating, for each sample period, to selective couple the bias current generator only for a first time duration so as to obtain for one of the sampling capacitors a final state of stable charge, the control circuit further operating to terminate selective coupling of the sampling capacitor to the bit line for the sample period a second time duration after termination of the first time duration.

32. (New) The circuit of claim 31, wherein the second time duration is chosen in such a way as to obtain at the end of the sample period, a residual current flowing through the follower transistor less than a threshold level of the noise of the follower transistor.

33. (New) The circuit of claim 32, wherein the threshold level for the noise of the follower transistor lies between approximately 50 and 100 microvolts.

34. (New) The circuit according to claim 31, wherein the first time duration is a fraction of a duration of the sample period.

35. (New) The circuit of claim 34, wherein the duration of the sample period is of the order of one microsecond and the first time duration is of the order of 100 nanoseconds.

36. (New) The circuit of claim 15, wherein the bias current generator is connected to the bit line by an interrupter circuit controlled by the control circuit.

37. (New) The circuit of claim 15, further comprising means for precharging each sampling capacitor to an initial value before each sample period.

38. (New) The circuit of claim 37, wherein each sampling capacitor includes a first and second terminals, wherein a first terminal is grounded, and the means for precharging comprise an interrupter circuit for each capacitor which selectively connects the second terminal of the sampling capacitor to ground.

39. (New) The circuit of claim 26, wherein the control circuit operating to selectively couple the bias current generator to the bit line further comprises operating, for the sample period, to selective couple the bias current generator only for a first time duration so as to obtain for the sampling capacitor a final state of stable charge, the control circuit further operating to terminate selective coupling of the sampling capacitor to the bit line for the sample period a second time duration after termination of the first time duration.

40. (New) The circuit of claim 39, wherein the second time duration is chosen in such a way as to obtain at the end of the sample period, a residual current flowing through the follower transistor less than a threshold level of the noise of the follower transistor.

41. (New) The circuit of claim 40, wherein the threshold level for the noise of the follower transistor lies between approximately 50 and 100 microvolts.

42. (New) The circuit according to claim 39, wherein the first time duration is a fraction of a duration of the sample period.

43. (New) The circuit of claim 42, wherein the duration of the sample period is of the order of one microsecond and the first time duration is of the order of 100 nanoseconds.

44. (New) The circuit of claim 26, wherein the bias current generator is connected to the bit line by an interrupter circuit controlled by the control circuit.

45. (New) The circuit of claim 26, further comprising means for precharging the sampling capacitor to an initial value before each sample period.

46. (New) The circuit of claim 45, wherein the sampling capacitor includes a first and second terminals, wherein a first terminal is grounded, and the means for precharging comprise an interrupter circuit which selectively connects the second terminal of the sampling capacitor to ground.